FLEX 10K Devices: The Density Leader

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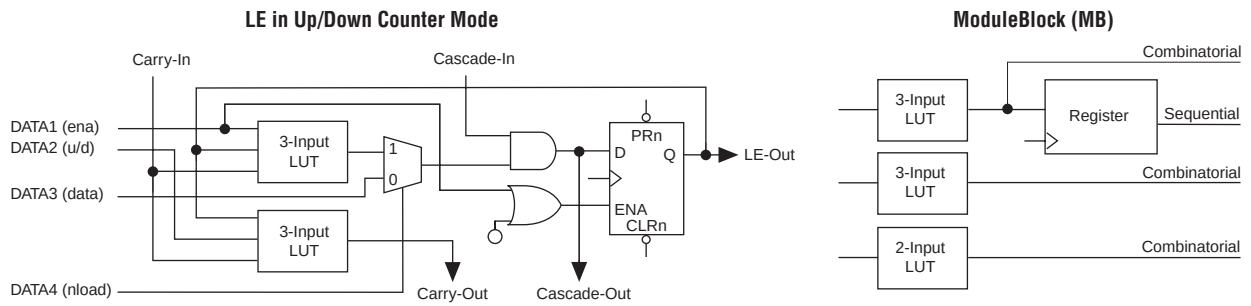
When designing a printed circuit board (PCB), many elements are considered before achieving the best design solution, e.g., device density, performance, price, and availability. FLEX® 10K devices are the density leader, but other features make these devices the time-to-market choice. This technical brief discusses key advantages of FLEX 10K devices compared with other high-density devices.

Device Density

Comparing densities among competing devices is not an easy task. For example, the basic building block of FLEX 10K devices is the logic element (LE), and Altera® specifies that each LE contains 12 usable gates. Similarly, the basic building block of Actel's embedded system (ES) system programmable gate array (SPGA) is the ModuleBlock (MB), and Actel specifies that each MB contains 16 usable gates. However, Altera Applications recently evaluated the MB and determined that the gate count between LEs and MBs is actually equal. Figure 1 shows the LE and MB: the only difference is the extra LUT in the MB and the extra AND gate and multiplexer in the LE. When counting usable gates, the extra LUT in the MB is of equal value to the extra AND gate and multiplexer in the LE. Thus, Actel's 100,000-gate device (A65ES100) is of comparable density to Altera's 70,000-gate device (EPF10K70).

Figure 1. LE & MB Architecture



In addition, the LE architecture offers the flexibility of four operating modes: normal, arithmetic, up/down counter, and clearable counter. During design configuration, MAX+PLUS® II assigns the most efficient operating mode, utilizing all four modes where appropriate. For example, if a design requires higher fan-in, the 4-input normal mode would be used. In contrast, the MB does not offer a 4-input alternative.

Performance & Price

The continuous routing structure of the FLEX 10K architecture provides fast and predictable routing delays. In contrast, Actel ES devices use a segmented routing structure; therefore, performance varies. Table 1 lists performance differences for the slowest speed grade EPF10K70 and A65ES100 devices. Altera Applications found similar differences when comparing faster speed grades.

Table 1. EPF10K70 & A65ES100 Performance

Device	Speed Grade	Clock-to-Output Delay (ns)	Register-to-Register Delay (ns), *Note (1)*	Benchmark Frequency (MHz), *Note (2)*
A65ES100	Standard	13.8, *Note (3)*	38.8 to 76.1	13.1 to 25.8
EPF10K70	-4	12.7, *Note (4)*	24.2	41.3

Notes to table:
(1) The register-to-register delay was obtained from the Actel *Reprogrammable SPGAs Preliminary Advance Information*, the Altera ***1996 Data Book***, and MAX+PLUS II.
(2) The benchmark frequency is the inverse of the register-to-register delay and represents the system clock frequency for an average application. The register-to-register path contains a register driving another register through three combinatorial LEs and some routing. In some applications, clock frequencies can reach much higher values.
(3) The Actel *Reprogrammable SPGAs Preliminary Advance Information* states that the A65ES100 -1 speed grade has a clock-to-output delay of 12 ns. Therefore, because Actel states that the A65ES100 -1 speed grade is 15% faster than the Standard speed grade, the clock-to-output delay is approximately (12 ns) X (1.15) = 13.8 ns.
(4) Source: Altera ***1996 Data Book***

Table 2 shows density, price, and routing differences for comparable FLEX 10K and ES SPGA devices.

Table 2. EPF10K70 & A65ES100 Device Density, Price, and Routing

Device	Speed Grade	Density, *Note (1)*	Price	Routing
A65ES100	Standard	73,000	$348, *Note (2)*	Segmented
EPF10K70	-4	72,000	$115, *Note (3)*	Continuous

Notes:
(1) Based on 12 usable gates per MB/LE.
(2) Volume price projection from the following Actel press release, *Actel Announces the Industry's First Family of System Programmable Gate Arrays; ES "System on a Chip" Family Offers Up to 400,000 Programmable Gates; Includes Embedded ASIC Cores*, October 21, 1996.
(3) End of 1997 volume price projection (North America OEM direct).

Availability

The most important time-to-market issue is availability. The FLEX 10K device family offers immediate availability, with densities ranging from 10,000 to 130,000 gates. As of this printing, Actel's high density device offering is not yet available. Table 3 lists FLEX 10K and ES SPGA device availability.

Table 3. FLEX 10K & ES SPGA Device Availability

FLEX 10K Device	Availability	ES SPGA Device	Availability, *Note (1)*
EPF10K70	Now	A65ES100	First half of 1997
EPF10K100	Now	A65ES150	Not disclosed
EPF10K130V	Now	A65ES200	Not disclosed

Note:
(1) Source: Actel press release, *Actel Announces the Industry's First Family of System Programmable Gate Arrays; ES "System on a Chip" Family Offers Up to 400,000 Programmable Gates; Includes Embedded ASIC Cores*, October 21, 1996.

The documents listed below provide more detailed information. The part numbers are in parentheses.

- *Gate Counting Methodology for Altera's FLEX 10K Family of Embedded Programmable Logic* (M-WP-GAEPLF-01)
- *FLEX 10K Embedded Programmable Logic Family Data Sheet* (A-DS-F10K-02)

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